1. For use with a home video game system having a game microprocessor for executing a first portion of a video game program, a game cartridge comprising:

a program memory for storing said first portion of said video game program and a second portion of said video game program, and

a programmable processing unit coupled to said program memory for executing said second portion of said video game program in response to signals received from said game microprocessor.

2. A game cartridge according to claim 1, further including a program memory bus coupled to said program memory and said programmable processing unit for transmitting address, data and control information; a random access memory unit, a random access memory unit bus, coupled to said random access memory unit and said programmable processing unit, for transmitting address, data and control information; and a game microprocessor bus for transmitting address, data and control information between said programmable processing unit and said game microprocessor.

3. A game cartridge according to claim 2, wherein said programmable processing unit includes means for controlling access to at least one of said program memory bus and said random access memory unit bus.

4. A game cartridge according to claim 3, wherein said means for controlling access includes

mode indicating register means for indicating whether the programmable processing unit has access to at least one of said program memory bus and said random access memory unit bus.

5. A game cartridge according to claim 1, wherein said programmable processing unit includes means for receiving address information from said game microprocessor for identifying the program memory location storing an instruction to be executed by the programmable processing unit.

6. A game cartridge according to claim 5, wherein said means for receiving address information includes a program memory bank register for receiving address information identifying a program memory bank and a program counter for identifying a location within said memory bank.

7. A game cartridge according to claim 1, wherein said programmable processing unit includes status register means for storing a plurality of programmable processing unit status indications including an indication that the programmable processing unit has sent an interrupt signal to the game microprocessor.

8. A game cartridge according to claim 1, wherein said programmable processing unit includes an arithmetic and logic unit for executing at least some of said second portion of instructions stored in said program memory and a plotting circuit for executing

at least one display related instruction stored in said program memory.

9. A game cartridge according to claim 8, wherein said plotting circuit includes a conversion circuit for converting pixel-based format data into character-based format data.

10. A game cartridge according to claim 9, wherein said plotting circuit includes buffering means for temporarily storing character-based format data generated by said conversion circuit.

11. A game cartridge according to claim 8, further including a first data source bus, a second data source bus and a data destination bus, each of said buses being coupled to said arithmetic and logic unit and said plotting circuit.

12. A game cartridge according to claim 1, wherein said programmable processing unit further includes a cache controller and a cache memory coupled to said cache controller, said programmable processing unit including means for executing instructions stored in said cache memory.

13. A game cartridge according to claim 12, further including an instruction bus and an arithmetic and logic means, coupled to said instruction bus, for executing instructions, said cache memory being coupled to said instruction bus and being operable to output instructions to said instruction bus.

14. A game cartridge according to claim 1, wherein said programmable processing unit includes a plurality of registers, said programmable processing unit further including means responsive to the accessing of a predetermined one of said plurality of registers for automatically initiating a program memory fetching operation.

15. A game cartridge according to claim 1, wherein said program memory is a read-only memory (ROM) for storing program instructions and display data and further including a random access memory (RAM) coupled to said programmable processing unit.

16. A game cartridge according to claim 1, wherein said programmable processing unit and said game microprocessor are operable to execute instructions in parallel.

17. A game cartridge according to claim 1, wherein said programmable processing unit includes a plurality of general registers and bus means for providing said game microprocessor access to said plurality of general registers.

18. A game cartridge according to claim 1, wherein said programmable processing unit includes means for pipelining instructions to be executed.

19. A game cartridge according to claim 1, wherein said programmable processing unit further includes means for decoding instructions from said second portion of said video game program and

look-ahead means for processing operation codes in advance of the associated instruction being decoded.

20. In an information processing system having a host processing unit for executing a videographics program stored at least in part in an external memory in an external memory system, said external memory system comprising:

at least one connector for coupling said external memory system to said host processing system;

an external memory for storing a first set of program instructions of said videographics program for execution by said host processing unit and for storing a second set of instructions of said videographics program; and

a graphics processor coupled to said external memory and coupled, in use, to said host processing unit via said at least one connector, for executing said second set of instructions.

21. An external memory system according to claim 20, wherein said host processing unit is a video game system main processing unit and said external memory system is embodied within a video game cartridge.

22. An external memory system according to claim 20, further including an external memory bus coupled to said external memory and said graphics processor for transmitting address, data and control information; a random access memory unit, a random access memory unit bus, coupled to said random access memory unit and said graphics processor, for

transmitting address, data and control information; and a host processing unit bus for transmitting address, data and control information between said graphics processor and said host processing unit.

23. An external memory system according to claim 22, wherein said graphics processor includes means for controlling access to at least one of said external memory bus and said random access memory unit bus.

24. An external memory system according to claim 23, wherein said means for controlling access includes mode indicating register means for indicating whether the graphics processor has access to at least one of said external memory bus and said random access memory unit bus.

25. An external memory system according to claim 20, wherein said graphics processor includes means for receiving address information from said host processing unit for identifying the external memory location storing an instruction to be executed by the graphics processor.

26. An external memory system according to claim 25, wherein said means for receiving address information includes an external memory bank register for receiving address information identifying an external memory bank and a program counter for identifying a location within said memory bank.

27. An external memory system according to claim 20, wherein said graphics processor includes status register means for storing a plurality of graphics processor status indications including an indication that the graphics processor is currently in operation.

28. An external memory system according to claim 27, wherein said status register means stores an indication that the graphics processor has sent an interrupt signal to the host processing unit.

29. An external memory system according to claim 20, wherein said graphics processor includes an arithmetic and logic unit for executing at least some of said second set of instructions stored in said external memory and a plotting circuit for executing at least one display related instruction stored in said external memory.

30. An external memory system according to claim 29, wherein said plotting circuit includes a conversion circuit for converting pixel-based format data into character-based format data.

31. An external memory system according to claim 30, wherein said plotting circuit includes buffering means for temporarily storing character-based format data generated by said conversion circuit.

32. An external memory system according to claim 29, further including a first data source bus, a second data source bus and a data destination bus,

each of said buses being coupled to said arithmetic and logic unit and said plotting circuit.

33. An external memory system according to claim 20, wherein said graphics processor includes a first data source bus, a second data source bus and a data destination bus.

34. An external memory system according to claim 20, said graphics processor further including a cache controller and a cache memory coupled to said cache controller, said graphics processor including means for executing instructions stored in said cache memory.

35. An external memory system according to claim 34, further including an instruction bus and an arithmetic and logic means coupled to said instruction bus for executing instructions, said cache memory being coupled to said instruction bus and being operable to output instructions to said instruction bus.

36. An external memory system according to claim 20, wherein said graphics processor includes a plurality of registers, said graphics processor further including means responsive to the accessing of a predetermined one of said plurality of registers for automatically initiating an external memory fetching operation.

37. An external memory system according to claim 20, wherein said external memory is a program

read-only memory (ROM) and further including a random access memory (RAM) coupled to said graphics processor.

38. An external memory system according to claim 20, wherein said graphics processor and said host processing unit are operable to execute instructions in parallel.

39. An external memory system according to claim 20, wherein said graphics processor includes a plurality of general registers and bus means for providing said host processing unit access to said plurality of general registers.

40. An external memory system according to claim 20, wherein said graphics processor includes means for pipelining instructions being executed.

41. An external memory system according to claim 20, wherein said graphics processor includes means for decoding said second set of instructions, and look-ahead means for processing operation codes in advance of the associated instruction being decoded.

42. An external memory system according to claim 20, wherein said information processing system includes a display for displaying an object and wherein said second set of instructions includes instructions for rotating said object, said graphics processor includes means for executing said instructions for rotating said object.

43. A video game system for use with a television type display comprising:

a game microprocessor for executing instructions of a video game program, and a picture processing unit coupled to said game microprocessor for performing picture processing tasks under the control of said game microprocessor;

a program memory for storing said video game program; and

a programmable graphics processor coupled to said program memory and connected in use to said game microprocessor for executing at least some of said video game program instructions.

44. A video game system according to claim 43, further including a program memory bus coupled to said program memory and said programmable graphics processor for transmitting address, data and control information; a random access memory unit, a random access memory unit bus, coupled to said random access memory unit and said programmable graphics processor for transmitting address, data and control information; and a game microprocessor bus for transmitting address, data and control information between said programmable graphics processor and said game microprocessor.

45. A video game system to claim 44, wherein said programmable graphics processor includes means for controlling access to at least one of said program memory bus and said random access memory unit bus.

46. A video game system according to claim 45, wherein said means for controlling access includes mode indicating register means for indicating whether the programmable graphics processor has access to at least one of said program memory bus and said random access memory unit bus.

47. A video game system according to claim 43, wherein said programmable graphics processor includes means for receiving address information from said game microprocessor for identifying the program memory location storing an instruction to be executed by the programmable graphics processor.

48. A video game system according to claim 47, wherein said means for receiving address information includes a program memory bank register for receiving address information identifying a program memory bank and a program counter for identifying a location within said memory bank.

49. A video game system according to claim 43, wherein said programmable graphics processor includes status register means for storing a plurality of programmable graphics processor status indications including an indication that the programmable graphics processor has sent an interrupt signal to the game microprocessor.

50. A video game system according to claim 43, wherein said programmable graphics processor includes an arithmetic and logic unit for executing at least some of said second portion of instructions stored in

said program memory and a plotting circuit for executing at least one display related instruction stored in said program memory.

51. A video game system according to claim 50, wherein said plotting circuit includes a conversion circuit for converting pixel-based format data into character-based format data.

52. A video game system according to claim 43, wherein said programmable graphics processor further includes a cache controller and a cache memory coupled to said cache controller, said programmable graphics processor including means for executing instructions stored in said cache memory, whereby said graphics processor and said game microprocessor are able to execute instructions in parallel.

53. A video game system according to claim 43, wherein said programmable graphics processor includes a plurality of registers, said graphics processor further including means responsive to the accessing of a predetermined one of said plurality of registers for automatically initiating a program memory fetching operation.

54. A video game system according to claim 43, wherein said graphics processor includes a plurality of general registers and bus means for providing said game microprocessor access to said plurality of general registers.

55. A video game system according to claim 43, wherein said game microprocessor and picture processing unit are embodied in a video game system main processing unit and said program memory and graphics processor are embodied within a video game cartridge.

56. For use in an information processing system having a first processing unit for executing at least a first portion of a videographics program stored in an external memory, a programmable graphics processor comprising:

means for receiving instructions from a second portion of said videographics program from said external memory; and

means for executing at least said second portion of said videographics programs.

57. A programmable graphics processor according to claim 56, wherein said information processing system further includes an external memory bus coupled to said external memory and said graphics processor for transmitting address, data and control information; a random access memory unit, a random access memory unit bus, coupled to said random access memory unit and said graphics processor, for transmitting address, data and control information; and a first processing unit bus for transmitting address, data and control information between said graphics processor and said first processing unit.

58. A programmable graphics processor according to claim 57, wherein said graphics processor includes

means for controlling access to at least one of said external memory bus and said random access memory unit bus.

59. A programmable graphics processor according to claim 58, wherein said means for controlling access includes mode indicating register means for indicating whether the graphics processor has access to at least one of said external memory bus and said random access memory unit bus.

60. A programmable graphics processor according to claim 56, further including means for receiving address information from said first processing unit for identifying the external memory location storing an instruction to be executed by the graphics processor.

61. A programmable graphics processor according to claim 60, wherein said means for receiving address information includes a external memory bank register for receiving address information identifying an external memory bank and a program counter for identifying a location within said memory bank.

62. A programmable graphics processor according to claim 56, wherein said graphics processor includes status register means for storing a plurality of graphics processor status indications including an indication that the graphics processor is currently in operation, and an indication that the graphics

processor has sent an interrupt signal to the first processing unit.

63. An external memory system according to claim 56, wherein said graphics processor includes an arithmetic and logic unit for executing at least some of said second portion of said videographics program stored in said external memory and a plotting circuit for executing at least one display related instruction stored in said external memory.

64. A programmable graphics processor according to claim 63, wherein said plotting circuit includes a conversion circuit for converting pixel-based format data into character-based format data.

65. A programmable graphics processor according to claim 63, further including a first data source bus, a second data source bus and a data destination bus, each of said buses being coupled to said arithmetic and logic unit and said plotting circuit.

66. A programmable graphics processor according to claim 56, further including a cache controller and a cache memory coupled to said cache controller, and means for executing instructions stored in said cache memory.

67. A programmable graphics processor according to claim 66, further including an instruction bus and an arithmetic and logic means, coupled to said instruction bus, for executing instructions, said cache memory being coupled to said instruction bus

and being operable to output instructions to said instruction bus.

68. A programmable graphics processor according to claim 56, further including a plurality of registers, and means responsive to the accessing of a predetermined one of said plurality of registers for automatically initiating an external memory fetching operation.

69. A programmable graphics processor according to claim 56, wherein said graphics processor is operable to execute instructions in parallel with said first processing unit.

70. A programmable graphics processor according to claim 56, wherein said graphics processor includes a plurality of general registers and bus means for providing said first processing unit access to said plurality of general registers.

71. A programmable graphics processor according to claim 56, wherein said graphics processor includes means for pipelining instructions being executed.

72. A programmable graphics processor according to claim 56, further including means for decoding instructions from said second portion of said videographics program and look-ahead means for processing instruction operation codes in advance of the associated instruction being decoded.

73. A programmable graphics processor according to claim 56, wherein said means for executing is operable to execute a prefix instruction, and an immediately following instruction, and wherein said prefix instruction serves to modify the operation initiated by said immediately following instruction.

74. A programmable graphics processor according to claim 56, wherein said information processing system includes a display for displaying an object and wherein said second portion of said videographics program include instructions for rotating said object, said means for executing being operable to execute said instructions for rotating said object.

75. A programmable processor comprising:

means for executing at least one instruction;

a status register for storing a plurality of status conditions;

an instruction decoder responsive to the state of at least one of said status conditions for causing said at least one instruction to control said means for executing to initiate a first operation if said status register is one state and for causing said means for executing to initiate a second operation if said status register is in a second state.

76. A programmable processor according to claim 75, wherein said first operation is an add operation and said second operation is an add with carry operation.

77. A programmable processor according to claim 75, wherein said status register is set to a predetermined state in response to a prefix instruction.

78. For use in an information processing system having a display for displaying at least one object and having a first processing unit for executing at least a first portion of a videographics program stored in an external memory, said external memory storing a second portion of said videographics program including instructions relating to rotating said object, a programmable graphics processor comprising:

means for receiving instructions from said second portion of said videographics program from said external memory; and

means for executing said instructions from said second portion of said videographics program, whereby said graphics processor coacts with said first processing unit to control rotation of displayed objects.

79. A programmable graphics processor according to claim 78, wherein said means for executing includes plotting circuitry for converting pixel-based format data into character-based format data.